EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(simulat$3.clm. WITH (verifi$6.clm. verify$3. clm.) WITH (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) same ((list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) WITH (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. WITH simulat$3.clm.)	US-PGPUB	OR	ON	2008/05/07 16:42

L2	0	(simulat$3.clm. WITH (verifi$6.clm. verify$3.clm.) WITH (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) same ((optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm. WITH (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) WITH (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model).clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. WITH simulat$3.clm.)	US-PGPUB	OR	ON	2008/05/07 16:43

L3	0	(simulat$3.clm. WITH (verifi$6.clm. verify$3.clm.) WITH (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) same ((optimize optimized optimizing optimization minimize minimized minimizing minimization reducing reduction reduced reduce resize resized resizing compaction compacting compacted redundancy redundant (timing ADJ shell) abstraction abstracted abstracting simplify simplification simplifying simplified) WITH (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) WITH (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model).clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. WITH simulat$3.clm.)	US-PGPUB	OR	ON	2008/05/07 16:47

L4	0	(simulat$3.clm. WITH (verifi$6.clm. verify$3. clm.) WITH (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) WITH (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. WITH simulat$3.clm.)	US-PGPUB	OR	ON	2008/05/07 16:57
L5	2	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) SAME (node net wire	US-PGPUB	OR	ON	2008/05/07 17:01

		gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME simulat$3.clm.)				
L6	2	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising). clm. SAME (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) SAME (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging	US-PGPUB	OR	ON	2008/05/07 17:05

		test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME simulat$3.clm.)				
L7	2	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((optimize optimized optimizing optimization minimize minimized minimizing minimization reducing reduction reduced reduce resize resized resizing compaction compacting compacted redundancy redundant (timing ADJ shell) abstraction abstracted abstracting simplify simplification simplifying simplified) SAME (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) SAME (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed	US-PGPUB	OR	ON	2008/05/07 17:08

		diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME simulat$3.clm.)				
L8	4	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((optimize optimized optimizing optimization minimize minimized minimizing minimization reducing reduction reduced reduce resize resized resizing compaction compacting compacted redundancy redundant (timing ADJ shell) abstraction abstracted abstracting simplify simplification simplifying simplified) AND (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) AND (node net wire gate logic cell block subblock sub$1block circuit sub $1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted	US-PGPUB	OR	ON	2008/05/07 17:11

		troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME simulat$3.clm.)				
L9	0	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((reconstruct reconstructed reconstructing reconstruction re $1construct re $1constructed re $1constructing re $1construction reassemble reassembled reassembling re $1assemble re $1assembled re $1assembling restore restored restoring restoration re$1store re $1stored re$1storing re $1storation) SAME (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) SAME (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot	US-PGPUB	OR	ON	2008/05/07 17:12

		troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME simulat$3.clm.)				
L10	1	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((reconstruct reconstructed reconstructing reconstruction re $1construct re $1constructed re $1constructing re $1construction reassemble reassembled reassembling re $1assemble re $1assembled re $1assembling restore restored restoring restoration re$1store re $1stored re$1storing re $1storation) SAME (NETLIST NET$1LIST RTL REGISTER $1TRANSFER$1LEVEL CIRCUIT ckt MICRO $1CIRCUIT ASIC MODEL logic)) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME simulat$3.clm.)	US-PGPUB	OR	ON	2008/05/07 17:12

L11	0	(simulat$3.clm. SAME (verifi$6.clm. verify$3. clm.) SAME (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((reconstruct reconstructed reconstructing reconstruction re $1construct re $1constructed re $1constructing re $1construction reassemble reassembled reassembling re $1assemble re $1assembled re $1assembling restore restored restoring restoration re$1store re $1stored re$1storing re $1storation) SAME (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) SAME (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm. SAME	US-PGPUB	OR	ON	2008/05/07 17:14

		simulat$3.clm.)				
L12	4	5 6 7 8 10	US-PGPUB	OR	ON	2008/05/07 17:16
L13	59	(simulat$3.clm. AND (verifi$6.clm. verify$3. clm.) AND (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor $3) NEAR data).clm.) AND (node net wire gate logic cell block subblock sub$1block circuit sub $1circuit subcircuit object module submodule sub $1module component subcomponent sub $1component model). clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm.)	US-PGPUB	OR	ON	2008/05/07 17:29

L14	30	(simulat$3.clm. AND (verifi$6.clm. verify$3.clm.) AND (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((reconstruct reconstructed reconstructing reconstruction re$1construct re$1constructed re$1constructing re$1construction reassemble reassembled reassembling re$1assemble re$1assembled re$1assembling restore restored restoring restoration re$1store re$1stored re$1storing re$1storation) AND (NETLIST NET$1LIST RTL REGISTER $1TRANSFER$1LEVEL CIRCUIT ckt MICRO $1CIRCUIT ASIC MODEL logic)) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble $1shoot trouble $1shooted trouble $1shooting).clm.)	US-PGPUB	OR	ON	2008/05/07 17:29

L15	0	(simulat$3.clm. AND (verifi$6.clm. verify$3.clm.) AND (optimize optimized optimization optimizing optimal optimum optimise optimised optimisation optimising).clm.) AND ((reconstruct reconstructed reconstructing reconstruction re$1construct re$1constructed re$1constructing re$1construction reassemble reassembled reassembling re$1assemble re$1assembled re$1assembling restore restored restoring restoration re$1store re$1stored re$1storing re$1storation) SAME (list listed listing enumerate enumerated enumeration enumerating database data$1base databank data$1bank (data adj repository) ((sav$3 stor$3) NEAR data).clm.) SAME (node net wire gate logic cell block subblock sub$1block circuit sub$1circuit subcircuit object module submodule sub$1module component subcomponent sub$1component model).clm.) and ((bug failure error mistake debug debugged debugging test tested testing check checked checking diagnose diagnosed diagnosing diagnosis diagnostics troubleshoot troubleshooted troubleshooting trouble$1shoot trouble$1shooted trouble$1shooting).clm.)	US-PGPUB	OR	ON	2008/05/07 17:29

L16	62	13 14	US-PGPUB	OR	ON	2008/05/07 17:30
L17	58	16 NOT 12	US-PGPUB	OR	ON	2008/05/07 17:30

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